WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of memory cells each of which includes a first MOS transistor with a charge accumulation layer and a control gate and a second MOS transistor which has one end of its current path connected to one end of a current path of the first MOS transistor;

a plurality of local bit lines each of which connects other ends of the current paths of the first MOS transistors;

a global bit line to which two or more of the local bit lines are connected in common;

a first switch element which makes a connection between the local bit lines and the global bit line; and

a holding circuit which is connected to the global bit line and holds data to be written into the memory cells.

2. The semiconductor memory device according to claim 1, further comprising:

word lines each of which connects the control gates of plurality of the memory cells in common, wherein

the data is written into the plurality of memory cells connected to the same one of the word lines are written into at the same time.

3. The semiconductor memory device according to

claim 1, wherein the data is written into the memory cells by exchanging electrons with the charge accumulation layer by FN tunneling.

4. The semiconductor memory device according to claim 1, further comprising:

a sense amplifier which amplifies read data, wherein

the global bit line includes a write global bit line and a read global bit line,

the first switch element includes a second switch which makes a connection between the write global bit line and the local bit lines and a third switch element which makes a connection between the read global bit line and the local bit lines,

the holding circuit is connected to the write global bit line, and

the sense amplifier is connected to the read global bit line.

5. The semiconductor memory device according to claim 4, wherein the third switch element includes

a third MOS transistor which has one end of its current path connected to the local bit lines and the other end of its current path, and

a fourth MOS transistor which has one end of its current path connected to the other end of the current path of the third MOS transistor, other end of its current path connected to the read global bit line and

a gate insulating film thinner than that of the third MOS transistor.

6. The semiconductor memory device according to claim 4, wherein the potential of the write global bit line is set at the ground potential in a read operation.

7. The semiconductor memory device according to claim 1, further comprising:

a sense amplifier which is connected to one end of the global bit line and amplifies read data; and

a third MOS transistor which has one end of its current path connected to the connection node of the local bit lines and the first switch element and the other end of its current path connected to a first potential, wherein

the holding circuit is connected to the other end of the global bit line, and

the gates of the third MOS transistors connected to the local bit lines sharing the global bit line are independent of one another.

8. The semiconductor memory device according to claim 1, further comprising:

a source line to which the other ends of the current paths of the second MOS transistors in the memory cells are connected in common; and

a source line driver which supplies a potential to the source line.

9. The semiconductor memory device according to claim 1, wherein a negative voltage is applied to the local bit lines in a write operation and a negative voltage is applied to the control gate of the first MOS transistor in an erase operation.

10. The semiconductor memory device according to claim 1, further comprising:

a plurality of cell blocks including two columns of the memory cells connected to two of the local bit lines respectively; and

a sense amplifier which amplifies the data read from the memory cells, wherein

each of the global bit lines includes two write global bit lines and one read global bit line,

the first switch element includes a second and a third switch element, and

in each of the cell blocks, two of the local bit lines are connected to the two write global bit lines via the second switch respectively and are connected to the one read global bit line via the third switch element in common,

the holding circuit is connected to each of the write global bit lines, and

the sense amplifier is connected to each of the read global bit lines.

11. The semiconductor memory device according to claim 1, further comprising:

a plurality of cell blocks including four columns of the memory cells connected to four of the local bit linesrespectively; and

a sense amplifier which amplifies the data read from the memory cells, wherein

each of the global bit lines includes two write global bit lines and one read global bit line,

the first switch element includes a second and a third switch element, and

in each of the cell blocks, two of the local bit lines are connected in common to one of the write global bit lines via the second switch element, the remaining two local bit lines are connected in common to the other of the write global bit lines via the second switch element, and the read global bit line is connected to all of the four local bit lines via the third switch element,

the holding circuit is connected to each of the write global bit lines, and

the sense amplifier is connected to each of the read global bit lines.

12. The semiconductor memory device according to claim 1, further comprising:

a plurality of cell blocks including two columns of the memory cells connected to two of the local bit lines respectively;

a second switch element which is provided for each

of the cell blocks and makes a connection between the two local bit lines and a first potential node; and

a sense amplifier which amplifies the data read from the memory cells, wherein

in each of the cell blocks, two of the local bit lines are connected in common to the global bit line via the first switch and, in a write operation, one of the local bit lines is connected to the global bit line by the first switch and disconnected from the first potential node by the second switch and the other of the local bit lines is connected to the first potential node by the second switch and disconnected from the global bit line by the first switch, and in a read operation, one of the local bit lines is connected to the global bit line by the first switch and the other of the local bit lines is disconnected from the global bit line by the first switch, and

the holding circuit is connected to one end of the global bit line and the sense amplifier is connected to the other end of the global bit line.

13. The semiconductor memory device according to claim 1, further comprising:

a plurality of cell blocks including four columns of the memory cells connected to four of the local bit lines respectively;

a second switch element which is provided for each of the cell blocks and makes a connection between the

four local bit lines and a first potential node; and

a sense amplifier which amplifies the data read from the memory cells, wherein

in each of the cell blocks, four of the local bit lines are connected in common to the global bit line via the first switch and, in a write operation, any one of the local bit lines is connected to the global bit line by the first switch and disconnected from the first potential node by the second switch and the remaining three local bit lines are connected to the first potential node by the second switch and disconnected from the global bit line by the first switch, and in a read operation, any one of the local bit lines is connected to the global bit line by the first switch and the remaining three local bit lines are disconnected from the global bit line by the first switch, and

the holding circuit is connected to one end of the global bit line and the sense amplifier is connected to the other end of the global bit line.

14. The semiconductor memory device according to claim 1, wherein the global bit line is made of a metal wiring layer located at the highest level in a memory cell array which has the memory cells arranged in a matrix.

15. A semiconductor memory device comprising:

a plurality of memory cells each of which includes

a first MOS transistor with a charge accumulation layer and a control gate;

word lines to which the control gates of two or more of the memory cells are connected in common, the data being written into two or more of the memory cells connected to the same word line at the same time by exchanging electrons with the charge accumulation layer by FN tunneling;

a plurality of local bit lines to which one end of a current path of the first MOS transistor of each of two or more of the memory cells is connected;

a global bit line to which two or more of the local bit lines are connected in common;

a first switch element which makes a connection between the local bit lines and the global bit line; and

a holding circuit which is connected to the global bit line and holds data to be written into the memory cells.

16. The semiconductor memory device according to claim 15, wherein each of the memory cells further includes a second MOS transistor which has one end of its current path connected to the other end of the current path of the first MOS transistor.

17. The semiconductor memory device according to claim 15, further comprising:

a sense amplifier which amplifies read data,

wherein

the global bit line includes a write global bit line and a read global bit line,

the first switch element includes a second switch which makes a connection between the write global bit line and the local bit lines and a third switch element which makes a connection between the read global bit line to the local bit lines,

the holding circuit is connected to the write global bit line, and

the sense amplifier is connected to the read global bit line.

18. The semiconductor memory device according to claim 17, wherein the third switch element includes a third MOS transistor which has one end of its current path connected to the local bit lines and the other end of its current path, and

a fourth MOS transistor which has one end of its current path connected to the other end of the current path of the third MOS transistor, the other end of the current path connected to the read global bit line and a gate insulating film thinner than that of the third MOS transistor.

19. The semiconductor memory device according to claim 17, wherein the potential of the write global bit line is set at the ground potential in a read operation.

20. The semiconductor memory device according to claim 15, further comprising:

a sense amplifier which is connected to one end of the global bit line and amplifies read data; and

a third MOS transistor has one end of its current path connected to the connection node of the local bit lines and the first switch element and the other end of its current path connected to a first potential, wherein

the holding circuit is connected to the other end of the global bit line, and

the gates of the third MOS transistors connected to the local bit lines sharing the global bit line are independent of one another.

21. The semiconductor memory device according to claim 15, further comprising:

a source line to which the other ends of the current paths of the second MOS transistors in the memory cells are connected in common; and

a source line driver which supplies a potential to the source line.

22. The semiconductor memory device according to claim 15, wherein a negative voltage is applied to the local bit lines in a write operation and a negative voltage is applied to the control gate of the first MOS transistor in an erase operation.

23. The semiconductor memory device according to

claim 15, further comprising:

a plurality of cell blocks including two columns of the memory cells connected to two of the local bit lines respectively; and

a sense amplifier which amplifies the data read from the memory cells, wherein

each of the global bit lines includes two write global bit lines and one read global bit line,

the first switch element includes a second and a third switch element, and

in each of the cell blocks, two of the local bit lines are connected to the two write global bit lines via the second switch element respectively, and the read global bit line is connected via the third switch element to the two local bit lines,

the holding circuit is connected to each of the write global bit lines, and

the sense amplifier is connected to each of the read global bit lines.

24. The semiconductor memory device according to claim 15, further comprising:

a plurality of cell blocks including four columns of the memory cells connected to four of the local bit lines respectively; and

a sense amplifier which amplifies the data read from the memory cells, wherein

each of the global bit lines includes two write

global bit lines and one read global bit line,

the first switch element includes a second and a third switch element, and

in each of the cell blocks, two of the local bit lines are connected in common to one of the write global bit lines via the second switch element, the remaining two local bit lines are connected in common to the other of the write global bit lines via the second switch element, and the read global bit line is connected to all of the four local bit lines via the third switch element,

the holding circuit is connected to each of the write global bit lines, and

the sense amplifier is connected to each of the read global bit lines.

25. The semiconductor memory device according to claim 15, further comprising:

a plurality of cell blocks including two columns of the memory cells connected to two of the local bit lines respectively;

a second switch element which is provided for each of the cell blocks and makes a connection between the two local bit lines and a first potential node; and

a sense amplifier which amplifies the data read from the memory cells, wherein

in each of the cell blocks, two of the local bit lines are connected in common to the global bit line

via the first switch and, in a write operation, one of the local bit lines is connected to the global bit line by the first switch and disconnected from the first potential node by the second switch and the other of the local bit lines is connected to the first potential node by the second switch and disconnected from the global bit line by the first switch, and in a read operation, one of the local bit lines is connected to the global bit line by the first switch and the other of the local bit lines is disconnected from the global bit line by the first switch, and

the holding circuit is connected to one of the global bit line and the sense amplifier is connected to the other end of the global bit line.

26. The semiconductor memory device according to claim 15, further comprising:

a plurality of cell blocks including four columns of the memory cells connected to four of the local bit lines respectively;

a second switch element which is provided for each of the cell blocks and makes a connection between the four local bit lines and a first potential node; and

a sense amplifier which amplifies the data read from the memory cells, wherein

in each of the cell blocks, four of the local bit lines are connected in common to the global bit line via the first switch and, in a write operation, any one

of the local bit lines is connected to the global bit line by the first switch and disconnected from the first potential node by the second switch and the remaining three local bit lines are connected to the first potential node by the second switch and disconnected from the global bit line by the first switch, and in a read operation, any one of the local bit lines is connected to the global bit line by the first switch and the remaining three local bit lines are disconnected from the global bit line by the first switch, and

the holding circuit is connected to one of the global bit line and the sense amplifier is connected to the other end of the global bit line.

27. The semiconductor memory device according to claim 15, wherein the global bit line is made of a metal wiring layer located at the highest level in a memory cell array which has the memory cells arranged in a matrix.

28. A semiconductor memory device comprising:

a plurality of memory cells each of which includes a first MOS transistor with a charge accumulation layer and a control gate and a second MOS transistor which has one end of its current path connected to one end of a current path of the first MOS transistor;

a plurality of cell blocks in each of which the memory cells are arranged in a matrix;

a memory cell array which has the cell blocks arranged in a matrix;

a plurality of local bit lines to which the other ends of the current paths of the first MOS transistors of the memory cells in the same column are connected in common in each of the cell blocks;

a plurality of global bit lines to which the local bit lines in the same column are connected in common in the memory cell array;

a first switch element which makes a connection between the local bit lines and the global bit lines; and

a holding circuit which is connected to each of the global bit lines and holds data to be written into the memory cells.

29. The semiconductor memory device according to claim 28, further comprising:

word lines to which the control gates of the memory cells in the same row are connected in common, wherein

the data is written into the plurality of memory cells connected to the same one of the word lines at the same time.

30. The semiconductor memory device according to claim 28, wherein the data is written into the memory cells by exchanging electrons with the charge accumulation layer by FN tunneling.

31. The semiconductor memory device according to claim 28, further comprising:

a sense amplifier which amplifies read data, wherein

the global bit lines include write global bit lines and read global bit lines,

the first switch element includes a second switch which makes a connection between the write global bit lines and the local bit lines and a third switch element which makes a connection between the read global bit lines and the local bit lines,

the holding circuit is connected to the write global bit lines, and

the sense amplifier is connected to the read global bit lines.

32. The semiconductor memory device according to claim 31, wherein the third switch element includes a third MOS transistor which has one end of its current path connected to the local bit lines and the other end of its current path, and

a fourth MOS transistor which has one end of its current path connected to the other end of the current path of the third MOS transistor, the other end of its current path connected to the read global bit lines and a gate insulating film thinner than that of the third MOS transistor.

33. The semiconductor memory device according to

claim 31, wherein the potential of the write global bit line is set at the ground potential in a read operation.

34. The semiconductor memory device according to claim 28, further comprising:

a sense amplifier which is connected to one end of the global bit line and amplifies read data; and

a third MOS transistor has one end of its current path connected to the connection node between the local bit lines and the first switch element and the other end of its current path connected to a first potential, wherein

the holding circuit is connected to the other end of the global bit line, and

the gates of the third MOS transistors connected to the local bit lines sharing the global bit line are independent of one another.

35. The semiconductor memory device according to claim 28, further comprising:

a source line to which the other ends of the current paths of the second MOS transistors in the memory cells are connected in common; and

a source line driver which supplies a potential to the source line.

36. The semiconductor memory device according to claim 28, wherein a negative voltage is applied to the local bit lines in a write operation and a negative

voltage is applied to the control gate of the first MOS transistor in an erase operation.

37. The semiconductor memory device according to claim 28, wherein the global bit lines are made of a metal wiring layer located at the highest level in the memory cell array which has the memory cells arranged in a matrix.